## REMARKS

Applicants thank the Examiner for acknowledging the claim for priority under 35 U.S.C. § 119 and receipt of the certified copy of the priority document.

Applicants also thank the Examiner for considering the references cited in the Information Disclosure Statements (papers no. 5 and 6) filed in this application.

Claim 1 has been rejected under 35 U.S.C. § 112 (first paragraph). Applicants have canceled claims 10 and 11 without disclaimer or prejudice. Therefore this rejection is now moot.

Claims 1-19 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Sung ('831) in view of applicants' admitted prior art. This rejection is respectfully traversed. For the following reasons it is respectfully submitted that claims 1-7, 9, and 12-21, being the claims presently in the application, patentably distinguish over the cited references.

The present invention relates to a semiconductor device of the so-called system-on-chip type, wherein a CMOS logic circuit and a DRAM are fabricated on a single semiconductor chip. One of the features of claim 1 is in the claimed steps of producing a DRAM embedded in the system-on-chip semiconductor device. A feature of the claimed combination is forming a capacitor dielectric film of the DRAM, after removing a part of polysilicon film over an interlayer film, to reside on a part of the remaining polysilicon film which will be used as a lower electrode of a capacitor. Those steps prevent the lower electrode and an upper electrode formed over the dielectric film from being short-circuited.

On the other hand, Sung discloses that a polysilicon layer 37 and a hemi-spherical grained (HSG), which is an optional element, are formed as a storage node of a capacitor structure. Next, on a surface of the polysilicon layer 37, a capacitor dielectric layer 38 is formed.

After that, a CMP procedure is performed, resulting in the storage node layer 37 and the capacitor dielectric layer 38 to reside only in storage node opening 36. See column 7, line 49 to column 8, line 8.

In the method disclosed in Sung, since the capacitor dielectric layer 38 is formed before separating the polysilicon layer 37 and the capacitor dielectric layer 38 into each of the storage node layers 37, the cut edges of the separated polysilicon layer 37 and the separated capacitor dielectric layer 38 are exposed. After that, a polysilicon layer 39, which is an upper electrode, is formed to be electrically connected to the exposed cut edge of the polysilicon layer 37 as the storage node layer as shown in FIGS. 18 and 19. Therefore, the completed capacitor does not work according to the disclosure of Sung as the upper and lower electrodes are shorted to each other.

Clearly nothing in Sung makes up the deficiencies of the admitted prior art and therefore even if the admitted prior art is combined with Sung, the present invention is not taught or suggested nor does it even suggest a solution to the problem solved by the method of claim 1. In fact and to the contrary, Sung rather than avoiding the shorting of the upper and lower electrodes, actually discloses that they are shorted (See FIG. 19).

New claims 20 and 21 distinguish over the cited references at least for the reasons given above. In addition, these claims further distinguish over the cited references by way of the additional limitations set forth therein.

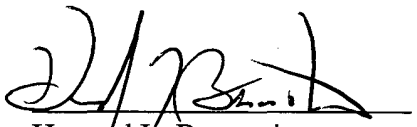
In view of the foregoing it is respectfully submitted that claims 1-7, 9, and 12-21 patentably distinguish over the prior art and are other wise in condition for allowance. It is

therefore respectfully requested that the subject application be passed to issue at the earliest possible time.

If for any reason the Examiner finds the application other than in condition for allowance he is respectfully requested to call the undersigned attorney at the Washington, D.C. telephone number 293-7060 to discuss the steps necessary for placing the application in condition for allowance.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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## APPENDIX
## VERSION WITH MARKINGS TO SHOW CHANGES MADE

**IN THE CLAIMS:**

**Claims 8, 10 and 11 are canceled.**

**The claims are amended as follows:**

1. (Amended) A method of manufacturing a system-on-chip semiconductor device, including a CMOS logic circuit [portion] and a DRAM [portion] on the same semiconductor chip, comprising the steps of:

providing a CMOSlogic circuit portion and a DRAM portion of a substrate;

forming [at least] a first transistor on [a]said substrate at said CMOS logic circuit portion;

forming [at least] a second transistor on said substrate at said DRAM portion;

forming an interlayer film on said substrate at said CMOS logic circuit portion and on said substrate at said DRAM portion, covering said [at least a] first transistor and said [at least a] second transistor;

forming a groove in said interlayer film by removing a portion of said interlayer film at said DRAM portion;

forming a first polysilicon film on an upper surface of said interlayer film at said CMOS logic circuit portion and at said DRAM portion, and a second polysilicon film on an inner wall of said groove at said DRAM portion,

forming a first HSG on a surface of said first polysilicon film and a second HSG on a surface of said second polysilicon film; [and]

removing said first HSG and said first polysilicon film

forming a capacitor dielectric film n said HSG after removing said first HSG and said first polysilicon film; and

forming an upper electrode on said capacitor dielectric film.

2.(Amended) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 1,

wherein said step of forming said [at least a] first transistor includes a step of forming a first gate insulating layer, and

wherein said step of forming said [at least a] second transistor includes a step of forming a second gate insulating layer,

wherein said first gate insulating layer is thinner that said second gate insulating layer.

3. (Amended) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 2,

wherein said [at least a] second transistor comprises a peripheral circuit transistor and a switching transistor, and

wherein said peripheral circuit transistor and said switching transistor have similar structures.

7. (Amended) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 6, further comprising steps of:

forming a first photoresist layer on said first HSG and a second [resist]photoresist layer on said second HSG; and

removing said first photoresist layer to expose said first HSG.

9. (Amended) The method of manufacturing a system-on-chip semiconductor device as claimed in claim [8]7, wherein said capacitor dielectric film comprises a Ta2O5 film[; and

further comprising a step of forming a TiN film on said Ta2O5 before said step of forming said upper electrode].

16. (Amended) A method of manufacturing a system-on-chip semiconductor device including a CMOS logic circuit [portion] and a DRAM [portion]on the same semiconductor chip, said DRAM [portion] comprising a cylinder type capacitor, the method comprising the steps of:

providing a CMOS logic circuit portion and a DRAM portion on a substrate;

forming a first transistor on a substrate at said CMOS logic circuit portion;

forming a second transistor on said substrate at said DRAM portion;

forming an interlayer film on said substrate at said CMOS logic circuit portion and on said substrate at said DRAM portion, covering said first transistor and said second transistor;

forming a groove in said interlayer film by removing a portion of said interlayer film at said DRAM portion;

forming a polysilicon film on [a] said interlayer film at said CMOS logic circuit portion and at said DRAM portion, and on [a]an inner wall of said groove at said DRAM portion,

forming [a]an HSG on a surface of said polysilicon film; [and]

removing said HSG and said polysilicon film from an upper surface of said interlayer film, retaining at least a portion of said HSG in said groove and at least a portion said polysilicon in said groove; and

forming a capacitor dielectric film on said portion of said HSG in said groove after removing said HSG and said polysilicon film.

17. (Amended) The method of manufacturing a system-on-chip semiconductor device as claimed in claim 16,

wherein said step of forming said [at least a] first transistor includes a step of forming a first gate insulating layer, and

wherein said step of forming said [at least a] second transistor includes a step of forming a second gate insulating layer,

wherein said first gate insulating layer is thinner that said second gate insulating layer.

**Claims 20 and 21 are added as new claims.**